REMARKS

Applicant has studied the Office Action dated July 2, 2003 and has made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. Claims 1-24 are pending. Claims 1, 3, 5, 6, 8-10, 12-14, 16-19, 23, and 24 have been amended. Reconsideration and allowance of the claims in view of the above amendments and the following remarks are respectfully requested.

Claims 1-24 were objected to because of the use of acronyms. The claims have been amended to express all acronyms in full form on first use. Applicant submits that all claims fulfill the requirements of 35 U.S.C. § 112. Therefore, it is respectfully submitted that the objection to claims 1-24 should be withdrawn.

Claims 1-7, 10-15, and 18-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chren, Jr. (U.S. Patent No. 5,430,764) in view of Arkin (U.S. Patent No. 5,917,834). This rejection is respectfully traversed.

The present invention is directed to residue number system (RNS) arithmetic circuits that have simple circuitry for performing built-in self testing of input-to-output (or propagation) delay. One embodiment of the present invention provides an arithmetic circuit for use with a Residue Number System (RNS). The arithmetic circuit includes an arithmetic core for performing an RNS arithmetic operation, test circuitry coupled to the arithmetic core, and logic circuitry coupled to the output of the arithmetic core. The test circuitry selectively feeds the output of the arithmetic core back to at least one of the inputs so as to induce oscillation at the output of the arithmetic core during testing.

The logic circuitry measures an oscillation frequency of the output of the arithmetic core during testing and produces a pass/fail signal to indicate whether or not the input-to-output delay of the arithmetic core is within specification. The pass/fail signal is based on a determination of whether the oscillation frequency is at least equal to a minimum threshold value. Thus, simple

built-in self test circuitry can be used to determine whether or not the propagation delay of the circuit is acceptable. Because timing verification is possible, the RNS arithmetic circuits of the present invention can be used in practical digital signal processing devices.

The Chren reference discloses digital frequency synthesizers that employ RNS-based processors to generate output waveforms. The Arkin reference discloses an integrated circuit tester having multiple period generators. However, neither Chren nor Arkin discloses an RNS arithmetic circuit that includes test circuitry that selectively feeds the output of an arithmetic core back to at least one of the inputs so as to induce oscillation at the output of the arithmetic core during testing, and logic circuitry that measures an oscillation frequency of the output of the arithmetic core during testing and produces a pass/fail signal to indicate whether or not the input-to-output delay of the arithmetic core is within specification based on whether the oscillation frequency is at least equal to a minimum threshold value, as is recited in amended claim 1. Amended claim 10 contains similar recitations.

Similarly, neither Chren nor Arkin discloses a method for testing propagation delay of an RNS arithmetic circuit in which the output of the arithmetic core is selectively fed back to one of the inputs of the arithmetic core and a constant is selectively provided to another input of the arithmetic core so as to induce oscillation at the output of the arithmetic core during testing, there is measured an oscillation frequency of the output of the arithmetic core during testing, and a pass/fail signal is produced to indicate whether or not the propagation delay of the arithmetic core is within specification based on a determination of whether the oscillation frequency is at least equal to a minimum threshold value, as is recited in amended claim 18.

As recognized by the Examiner, the Chren reference fails to disclose test circuitry for inducing oscillation at the output of the arithmetic core and logic circuitry producing a pass/fail signal. However, the Examiner went on to state that the Arkin reference makes up for this deficiency in the disclosure of Chren by disclosing such features. This position of the Examiner is respectfully traversed.

Arkin discloses a integrated circuit tester 10 that is connected between a host computer 24 and an integrated circuit 12 that is being tested. The tester 10 includes a channel CH(n) for each pin of the integrated circuit 12 being tested. Each of the channels CH(n) includes timing

circuitry, logic circuitry, and driving circuitry for delivering high and low logic levels to selected input pins and reading the logic levels of selected output pins at specified timings during testing. The tester 10 further includes a pattern generator 22 that receives test data from the host computer 24.

Based on the received test data, the pattern generator 22 generates control signals for each of the channels CH(n) so as to produce a desired pattern of input signals on the input pins during the testing. The pattern generator 22 also monitors each of the channels CH(n) for incorrect output signals on the output pins in response to the input signal pattern supplied to the input pins. Thus, the integrated circuit tester of Arkin directly supplies a predetermined pattern of input signals to the inputs of the circuit being tested, and monitors the resulting output signals each period to determine whether those output signals are proper for the input signal pattern that was supplied.

In contrast, in embodiments of the present invention, oscillation is induced at the output of an arithmetic core and there is measured an oscillation frequency of the output of the arithmetic core to determine whether or not the input-to-output delay of the arithmetic core is within specification. More specifically, the test circuitry selectively feeds the output of the arithmetic core back to at least one of the inputs of the arithmetic core so as to induce oscillation at the output of the arithmetic core during testing. The logic circuitry measures an oscillation frequency of the output of the arithmetic core during testing and produces a pass/fail signal to indicate whether or not the input-to-output delay of the arithmetic core is within specification, based on a determination of whether the oscillation frequency is at least equal to a minimum threshold value. Thus, in embodiments of the present invention, oscillation is induced at the output of the arithmetic core during testing by feeding the output of the arithmetic core back to one of the inputs of the arithmetic core, and there is measured an oscillation frequency of the output of the arithmetic core to determine whether or not the propagation delay of the arithmetic core is within specification.

Neither Chren nor Arkin teaches or suggests a circuit or method in which oscillation is induced at the output of an arithmetic core during testing by feeding the output of the arithmetic core back to one of the inputs of the arithmetic core, and there is measured an oscillation

frequency of the output of the arithmetic core to determine whether or not the propagation delay of the arithmetic core is within specification. These claimed features of the present invention allow simple built-in self test circuitry to be used to determine whether or not the propagation delay of the circuit is within specification. In particular, because the oscillation frequency is inversely proportional to the propagation delay between the input and output of the arithmetic core, the minimum threshold can be used o determine whether the propagation delay of the arithmetic core is acceptable. Because timing verification is possible, the RNS arithmetic circuits of the present invention can be used in practical digital signal processing devices.

Applicant believes that the differences between Chren, Arkin, and the present invention are clear in amended claims 1, 10, and 18, which set forth various embodiments of the present invention. Therefore, claims 1, 10, and 18 distinguish over the Chren and Arkin references, and the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

Claims 8, 9, 16, 17, 23, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chren, Jr. in view of Applicant's Admitted Prior Art ("AAPA"). This rejection is respectfully traversed.

As discussed above, claims 1, 10, and 18 distinguish over the Chren reference. Furthermore, the claimed features of the present invention are not realized even if the teachings of the AAPA are incorporated into Chren. The AAPA does not teach or suggest the claimed features of the present invention that are absent from Chren. Thus, claims 1, 10, and 18 distinguish over Chren and the AAPA, and thus, claims 8 and 9, claims 16 and 17, and claims 23 and 24 (which depend from claims 1, 10, and 18, respectively) also distinguish over Chren and the AAPA. Therefore, it is respectfully submitted that the rejection of claims 1, 8-10, 16-18, 23, and 24 under 35 U.S.C. § 103(a) should be withdrawn.

Applicant has examined the references cited by the Examiner as pertinent but not relied upon. It is believed that these references neither disclose nor make obvious the invention recited in the present claims. In view of the foregoing, it is respectfully submitted that the application

and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

Date: January 2, 2004

By: _____
Stephen Bongini
Registration No. 40,917
Attorney for Applicant

FLEIT, KAIN, GIBBONS,
GUTMAN, BONGINI & BIANCO P.L.
One Boca Commerce Center
551 Northwest 77th Street, Suite 111
Boca Raton, Florida 33487
Telephone: (561) 989-9811
Facsimile: (561) 989-9812